REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

Claims 1 and 3-5 are pending, with Claims 1, 3, and 5 having been amended and Claim 2 having been cancelled without prejudice or disclaimer.

In the outstanding Office Action, Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,687,796 to Laine and Claims 2-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Laine in view of U.S. Patent No. 6,728,795 to Farazmandnia.

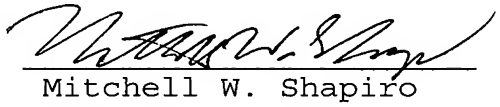
Without acceding to the rejection, Claim 1 has been amended to include the subject matter of Claim 2 (now cancelled). Claim 1 now sets forth that the direct memory access controller sets a number larger than the number of data received at a time as a number of transfers, and when the number of data transferred from a serial interface to a first memory reaches the number set as the number of transfers, the direct memory access controller outputs a direct memory access transfer end interrupt signal to a central processing unit. It is apparent that Laine and Farazmandnia, whether taken or in combination, fail to teach or suggest the above-noted feature of amended independent Claim 1.

Laine is silent with respect to the above-noted features, nor does the Examiner rely on Laine for this teaching. Farazmandnia fails to cure this deficiency in Laine because Farazmandnia merely discloses a direct memory access ("DMA") controller 206 and DMA FIFO 204, wherein the DMA FIFO 204 can be any size, and once the DMA FIFO 204 is filled with x valid bytes, the data from the DMA FIFO 204 is transferred over a bus by DMA controller 206 to a host memory 208 or protocol stack. *See* Farazmandnia, col. 3, lines 24-38; Figure 2. Thus, Farazmandnia fails to teach or suggest that the direct memory access controller sets a number larger than the number of data received at a time as a number of transfers, as recited in amended independent Claim 1. It therefore follows that Farazmandnia fails to suggest that when the number of data transferred from the serial interface to the first memory reaches the number (set by the DMA controller) as the number of transfers, the direct memory access controller outputs a direct memory access transfer end interrupt signal to a central processing unit. Accordingly, Claim 1 is patentable over the applied references and should be allowed. Claims 3-5 are allowable at least based on their dependence from Claim 1.

In view of the foregoing, Applicants respectfully request a Notice of Allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10061) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By: 

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January 29, 2007